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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,462	04/02/2004	John R. Beers	200312363-1	3193

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HEWLETT PACKARD COMPANY  
P O BOX 272400, 3404 E. HARMONY ROAD  
INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER

HOANG, HUAN

ART UNIT PAPER NUMBER

2827

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/817,462

Applicant(s)

BEERS ET AL.

Examiner

Huan Hoang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 7-13, 15, 16, 19-21 and 24-27 is/are rejected.
- 7) ☒ Claim(s) 4-6, 14, 17, 18, 22, 23, 28 and 29 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 040204.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 7, 8, 10-13 and 24-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata.

Iwata discloses a storage device having all the elements and steps as recited in claims 1-3, 7, 8, 10-13 and 24-27 as follows:

a plurality of groups of memory cells (a plurality of columns of cells, Fig. 3);

wherein each group further includes a corresponding transistor (SW, Fig. 3), and the memory cells of each group includes a first set of parallel connected memory cells connected to a node of the transistor; and a sensing device (29, Fig. 3) to detect a state of a memory cell in a selected one of the groups (column 10, lines 7-13);

wherein each group further comprises a second set of parallel connected memory cells (second groups of cells below the top group of cells connected to BL0, Fig. 17);

wherein the first set of memory cells comprises memory cells coupled in parallel between a first bias signal (Vss, Fig. 17) and a common node (drain/source of transistor

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SW), and wherein the second set of memory cells comprises memory cells coupled in parallel between a second bias signal ( $V_{ss}$ , Fig. 17);

a row decoder (25, Fig. 17) and a column decoder (21, Fig. 1);

wherein each memory cell is formed of a stack of layers (column 26, lines 36-41);

selecting at least one of a plurality of groups of memory cells, wherein each group of memory cells includes a first set of memory cells connected in parallel and a second set of memory cells connected in parallel, the first and second sets of memory cells connected to a common node (Fig. 17);

detecting a voltage at the common node of the selected group of memory cells (column 26, lines 2-8);

outputting an indicator of data state in response to the detected voltage of the node (output of the sense circuit 29)

writing a first cell to a first state;

measuring a second voltage at the common node; and

determining whether the first voltage differs from the second voltage, wherein outputting the indicator is based on a difference between the first and second voltages (column 3, lines 53-62).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 9, 15, 16 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata.

Iwata discloses all the limitations of claims 15, 16 and 19-21 (Fig. 3 and Fig.17) except for a processor couple to the storage device and sensing devices coupled to respective bit lines. However, a processor coupled to a memory device and sensing devices coupled to respective bit lines are well-known in the art to provide commands and instructions for the memory device and to sense data from a selected bit line in a memory device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a processor coupled to the memory device and sensing devices couple to respective bit lines to provide commands and instructions for the memory device and to sense data from a selected bit line in a memory device.

#### ***Allowable Subject Matter***

5. Claims 4-6, 14, 17, 18, 22, 23, 28 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or suggest the following:

wherein the common node is connected to a gate of the transistor, and wherein the source of the transistor is coupled to the sensing device.

wherein the transistor forms a pass gate, a first source/drain node of the transistor connected to the common node, a second/drain node of the transistor connected to the bit line, and a gate of the transistor connected to a select signal.

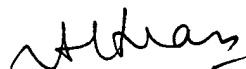
Wherein the transistor is a field effect transistor configured as a source follower or a bipolar transistor junction transistor configured as an emitter follower amplifier.

the steps as recited in claim 28.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Mon-Fri 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Huan Hoang  
Primary Examiner  
Art Unit 2827

HH  
7/7/05.